This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claims 1-16 (Cancelled)

17. (New) An integrated circuit (IC) comprising:

an after package trim circuit; and

a pin during a first time interval utilized by said after package trim circuit for a first function, said pin released by said after package trim circuit after said first time interval to make said pin available during a second time interval to said IC for a second function.

18. (New) The IC of claim 17, wherein said pin receives a common voltage signal during said first time interval.

19. (New) The IC of claim 17, wherein said after package trim circuit generates a trim voltage signal to add to an initial voltage reference signal generated by said IC.

20. (New) The IC of claim 19, wherein said after package trim circuit comprises:

an after-package trim cell circuit array adapted to provide a digital signal representative of a test signal; and

an output decision circuit adapted to receive said digital signal and provide an analog voltage reference signal at an output pin of said IC, said analog voltage reference signal equal to said trim voltage signal plus said initial voltage reference signal.

21. (New) An after package trim circuit comprising:

a trim cell circuit array adapted to receive a varying test signal and provide a trim cell circuit array digital signal in response to said test signal; and

an output decision circuit adapted to receive said trim cell array digital signal and provide a trimmed reference signal in response thereto, said after package trim cell circuit array further responsive to an input signal representative of said trimmed reference signal within a predetermined range of a high precision reference signal to set said trim cell circuit array digital signal equal to a value of said test signal that resulted in said trimmed reference signal within said predetermined range of said high precision reference signal.

22. (New) The circuit of claim 21, wherein said test signal comprises a sequential binary signal.

23. (New) The circuit of claim 21, wherein said output decision circuit comprises: a digital to analog converter (DAC) to receive said trim cell array digital signal and provide an analog trim current signal representative of said trim cell array digital signal; and a resistive element to convert said analog trim current signal into a trim voltage signal which when added to an initial voltage reference signal equals said trimmed reference signal.

24. (New) The circuit of claim 21, further comprising a register to provide said test signal.

25. (New) The circuit of claim 24, wherein said register is isolated from said trim cell circuit array in response to said input signal representative of said trimmed reference signal within a predetermined range of said high precision reference signal.

26. (New) The circuit of claim 25, further comprising an isolation trim cell circuit responsive to said input signal to isolate said register from said trim cell circuit array.

27. (New) A method comprising:

trimming an element of an integrated circuit (IC) utilizing a pin of said IC; and

releasing said pin for use by said IC after said trimming operation.

28. (New) The method of claim 27, wherein said pin receives a common voltage signal during said trimming operation.

29. (New) The method of claim 27, wherein said element comprises a reference voltage level.

30. (New) The method of claim 29, wherein said trimming operation comprises:

generating a binary test signal sequence;

generating a trim current representative of said binary test signal sequence at an output terminal;

generating a trim voltage from a resistive element coupled to said output terminal;

adding said trim voltage to a reference voltage to obtain a sum;

determining if said sum is within a predetermined range of a high precision reference signal; and

fixing said trim voltage if said sum is within said predetermined range.